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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,879	02/05/2004	Shinichi Amemiya	16UL02118	5548

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EXAMINER	
ROZANSKI, MICHAEL T	
ART UNIT	**PAPER NUMBER**
3768	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/772,879	AMEMIYA, SHINICHI	
	Examiner	Art Unit	
	Michael Rozanski	3768	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed February 5, 2004 have been fully considered but they are not persuasive.

After further consideration of the response and amendment, examiner respectfully disagrees with the applicant. Examiner would like to point out that all claimed features including the bias power source generating circuit that includes at least one diode and at least one capacitor. Specifically, Ramos Fernandez et al. describe rectifier sets GR1 and GR2 (as noted in applicant remarks) being implemented by means of two diode networks RD1 and RD2 (col. 4, lines 66-67). Further, the circuit includes a series of capacitors (col. 4, lines 47-55). Therefore, Ramos Fernandez et al. disclose all claimed features in claim 1 as described from the previous office action dated December 14, 2006 and incorporated below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Ramos Fernandez et al. (US Patent No. 5,592,031). Ramos Fernandez et al. are descriptive of

a pulse-echo system for medical echography (Col. 1, line 30), such as ultrasound imaging. The reference teaches that high voltage analog switches for the transducer pulse sources may be configured to operate with bidirectional behavior within multi-channel arrays and that the high voltage transmitter power source itself includes high voltage analog switches powered by the high voltage (Col. 4, lines 18-43). The transmitter power source that controls the analog switch is under low voltage TTL external control of the switch CBT (Col. 3, lines 25-34). Therefore, the system described by Ramos Fernandez et al. includes a low voltage source controlled by TTL logic circuits that powers high voltage pulses that, in turn, power high voltage analog switches. The analog switch also acts to directly power the transducer(s) (col. 1, line 51 – col. 2, line 8). In the same field of endeavor, Ramos Fernandez et al. describe rectifier sets GR1 and GR2 (as noted in applicant remarks) being implemented by means of two diode networks RD1 and RD2 (col. 4, lines 66-67). Further, the circuit includes a series of capacitors (col. 4, lines 47-55).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 4, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barnes et al. (US Patent No. 6,795,374) in view of Ramos Fernandez et al. In

reference to claim 1, Barnes et al. discloses an ultrasonic diagnostic apparatus (Fig. 1, element 10) for transmitting ultrasonic signals from ultrasonic transducers 68 toward a subject to be examined, and receiving reflected waves of said ultrasonic signals for display, comprising: An analog switch 14 for switching ultrasonic transducers for transmission of said ultrasonic signals and reception of said reflected waves; a transmitter power source 100 for supplying a high voltage to a transmitter circuit for causing said ultrasonic transducers to drive said ultrasonic signals; and a bias power source generating circuit (see Fig. 4) for generating a bias power source for said analog switch 14 from said transmitter power source 100.

In reference to claim 2, Barnes et al. discloses a bias voltage that is "reduced for transmission and then increased for reception" (Col. 8, lines 7-8). It follows in Col. 8, lines 8-25 that the bias voltage source generating circuit (see Fig. 4) is able to generate a voltage value higher than a positive voltage value of the transmitter power source 100 and a voltage lower than a negative voltage value of the transmitter power source 100. Barnes et al. also discloses how the polarity of the bias voltage is reversed between sub-elements 94 and 96 in the micro-mechanical ultrasound element, or MUT 68. There is both a positive node and a negative node of the bias voltage source capable of outputting a voltage higher than the positive voltage of transmitter power source and a voltage lower than the negative voltage of the transmitter power source (Col. 11, lines14-19).

In reference to claim 4, Barnes et al. discloses the ultrasonic diagnostic apparatus 10 of claim 1, wherein said apparatus is a transmission voltage control circuit

(see Figs. 2 and 4) for variably controlling the voltage value of said transmitter power source 100. Specifically, Barnes describes a transducer in which the DC supply 100, or transmitter power source, is "programmable or at least provides selectable DC voltage levels" (Col. 5, lines 41-45). Therefore, the reference includes a transmission voltage control circuit for adjusting the transmitter power source voltage value.

In reference to claim 6, Barnes et al. discloses the ultrasonic diagnostic apparatus 10 of claim 1, wherein said transmitter power source 100 comprises a stabilizing power source circuit (see Figs. 2 and 4) that is capable of decreasing and stabilizing the positive voltage value supplied to said transmitter circuit, and a stabilizing power source circuit for increasing and stabilizing the negative voltage value supplied to said transmitter circuit. The DC supply 100 includes selectable DC voltage levels, which may be used in stabilizing the voltage value in combination with the change in bias voltage 56.

However, Barnes et al. do not disclose at least one diode and at least one capacitor. In the same field of endeavor, Ramos Fernandez et al. describe rectifier sets GR1 and GR2 (as noted in applicant remarks) being implemented by means of two diode networks RD1 and RD2 (col. 4, lines 66-67). Further, the circuit includes a series of capacitors (col. 4, lines 47-55). Therefore, it would have been obvious to one with ordinary skill in the art at the time the invention was made to incorporate a diode and capacitor in order to improve the control over the flow of electric energy.

6. Claims 3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barnes et al. in view of Ramos Fernandez et al., and in view of Sato el al. (US Patent 5,469,484). Barnes et al. teaches all the elements of the current invention, except for a circuit for generating the bias power source with at least one diode and at least one capacitor from the transmitter power source which is a charge pump. Ramos Fernandez et al. describe rectifier sets GR1 and GR2 (as noted in applicant remarks) being implemented by means of two diode networks RD1 and RD2 (col. 4, lines 66-67). Further, the circuit includes a series of capacitors (col. 4, lines 47-55). In the same field of endeavor, Sato et al. teaches a driver that includes "a booster circuit for receiving the first and second voltages and for providing a third voltage higher than the second voltage (Col. 2, lines 42-45). Similarly, Sato et al. teaches a "desirable substrate voltage Vsub as a reference voltage Vref, in which the boosted voltage obtained from the booster circuit 16 is used as the operation voltage thereof" (Col. 5, lines 22-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make use of a charge pump, or booster circuit, to provide power supply to the bias power source from the transmitter power source. This would serve to diminish the power loss from the voltage supply.

In reference to claim 5, Barnes et al. do not teach that the charge pump and the transmitter power source share a driving circuit. However, Sato et al. teaches of "a driver means for the solid-state imaging device, including a driving circuit for driving the video signal output means in response to the timing signal" and "a booster circuit for receiving the first and second voltages and for providing a third voltage higher than the

second voltage as a third output...wherein the driving circuit, the booster circuit, and the voltage setting means are formed on, or in the same semiconductor substrate" (Col. 2, lines 40-49). The said driver includes a driving circuit, which is analogous to a transmitter power source, and a booster circuit. Similarly, Sato et al. teaches of a register drive circuit 9 that includes a booster circuit 16 for boosting the VH voltage and a substrate voltage setting circuit 17 for setting a desirable substrate voltage to be applied to the CCD image sensor 1 (Col. 4, lines 57-61). In this sense, the booster circuit, or charge pump, shares a drive circuit with a substrate voltage setting circuit, analogous to a transmitter power source. Therefore, it would have been obvious to one of ordinary skill in the art to include a common driving circuit to both the charge pump and the transmitter power source. This would aid in decreasing the size of the power supply.

With respect to claim 6, Barnes et al. discloses a stabilizing power source circuit (see Figs. 2 and 4). The teachings of Sato et al. serve to show that it would have been obvious to one of ordinary skill in the art to include a stabilizing power source circuit for decreasing an stabilizing the positive value supplied to said transmitter circuit, and stabilizing power source circuit for increasing and stabilizing the negative value supplied to said transmitter circuit (col. 1, line 61 – col. 2, line 49). The boosted voltage of the booster circuit 16 is used as the power source voltage (see Col. 4, lines 62-63). Pump circuits are, by nature, stabilized power supplies and it would have been obvious to incorporate them to stabilize the voltage value supplied to the transmitter circuit.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The balance of art is cited to show ultrasound systems with bias and/or transmitter power sources and switches.

US Patent No. 6,645,145 to Dreschel et al. discloses an ultrasound system with bias voltage control 12a and micro-mechanical switch 90.

US Patent No. 6,328,697 to Fraser discloses a cMUT ultrasonic transducer with a charge source 30 and bias terminal 24.

US Patent No. 6,572,546 to Bax et al. discloses a high voltage supply 308, a low voltage supply 310, and a switch 302.

US Patent No. 4,563,899 to Nakamura discloses a power source 25, a voltage controller 26, and a pulsar 24.

US Patent No. 6,635,018 to Kawagishi et al. discloses ultrasonic diagnosis apparatus with an ultrasonic probe 12, a pulsar/preamplifier unit, and a transmission control section 22.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rozanski whose telephone number is 571-272-1648. The examiner can normally be reached on Monday - Friday, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eleni Mantis-Mercader can be reached on 571-272-4740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MR

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SPE ART UNIT 3768